IDEC Chip Design Contest

A 9V-Tolerant 71.4%-Efficiency Stacked-Switched-Capacitor Stimulation System with Level-Adaptive Switching Control and Rapid Stimulus-Synchronized Charge Balancing

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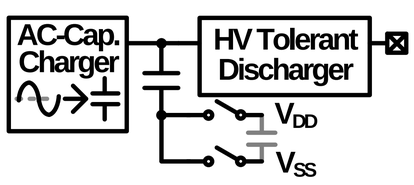
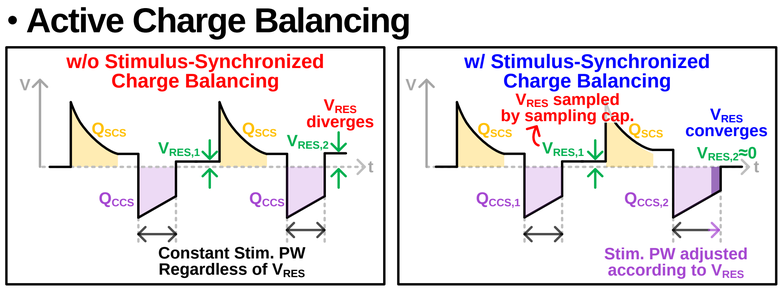
Concept of Proposed Idea

• **High-Voltage Tolerance**

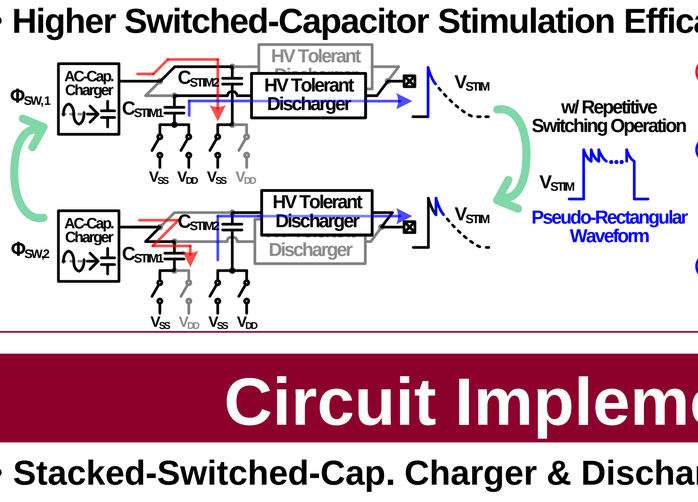


• **Active Charge Balancing**



-HV stimulation required for various applications and electrode compatibility.
☺ For HV range(0-V_{DD}) stimulation cap. stacked on V_{DD}.
-Active charge balancing w/o predefined step size and additional period required.
☺ Stimulation pulse width adjusted for charge matching.

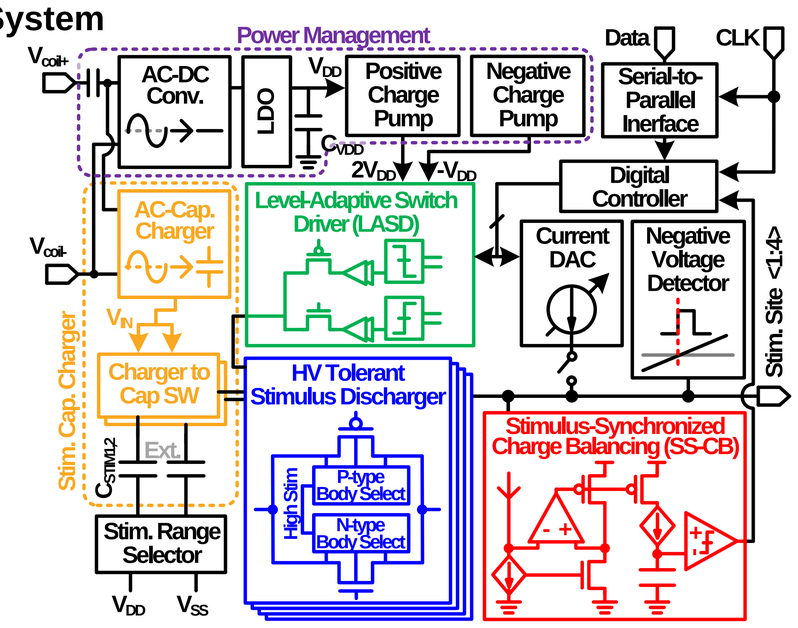
• **Higher Switched-Capacitor Stimulation Efficacy**



☹ Basic switched-cap. stimulation : decaying exponential waveform
☺ Periodically switching stim. cap. : sustains stimulation voltage level at target level
☺ Pseudo-rectangular waveform for higher efficacy.

Architecture of Proposed System

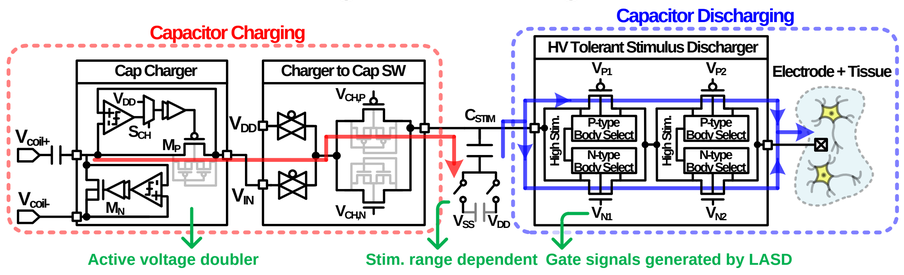
• **SSCS System**



☺ 4 Stimulation sites
☺ High-voltage ($2V_{DD}$) tolerant
☺ Wireless power & cap. charging
☺ 0-$2V_{DD}$ Stimulation range
☺ Stimulus-synchronized charge balancing
☺ Pseudo-rectangular stimulation waveform
☺ SPI & Full-Custom Digital Controller

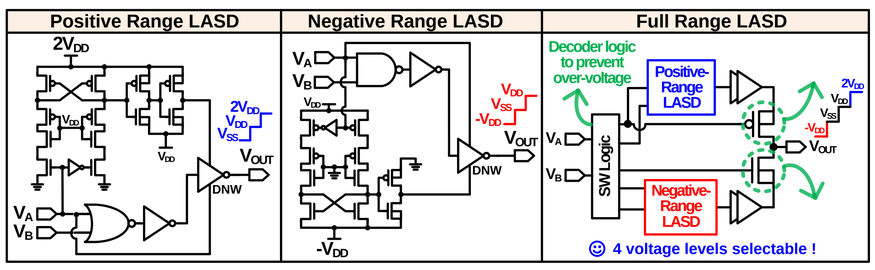
Circuit Implementation

• **Stacked-Switched-Cap. Charger & Discharger**



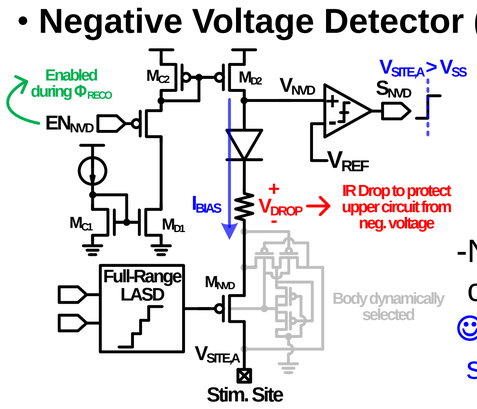
☺ Cap. charged through active diode : high charging efficiency
☺ Cap. discharged through cascaded switches for high-voltage tolerance.
☺ Switch controlled using level-adaptive switch drivers .

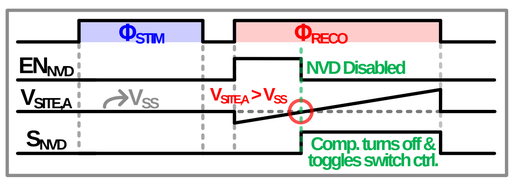
• **Level-Adaptive Switch Driver (LASD)**



☺ 2bit logic input to multi-level voltage output.
☺ LASD type selected and implemented based on each switch operation range.

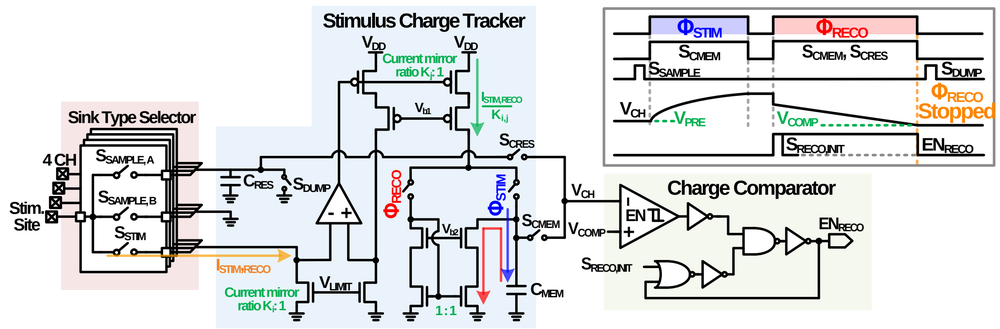
• **Negative Voltage Detector (NVD)**





-Neg. voltage might appear at stimulation site due to charged electrode capacitance.
☺ Detects neg. voltage and controls LASD and switches to prevent leakage and over-voltage problems.

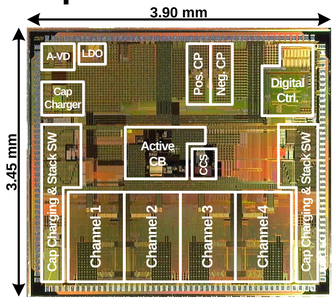
• **Stimulus-Synchronized Charge Balancer**



- Retrieves stimulation current to track transferred charge, and samples residual charge.
☺ 2nd biphasic phase PW controlled
☺ Transferred charge matched between biphasic phases.

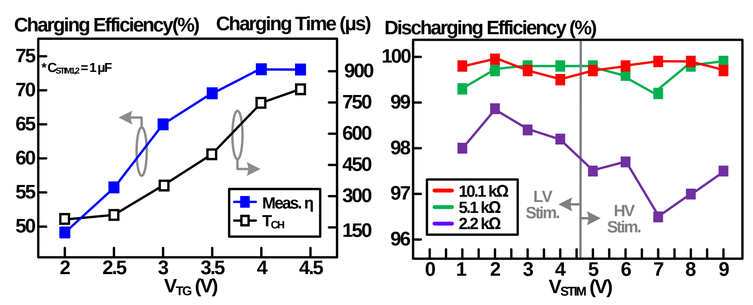
Measurement Results

• **Implementation**



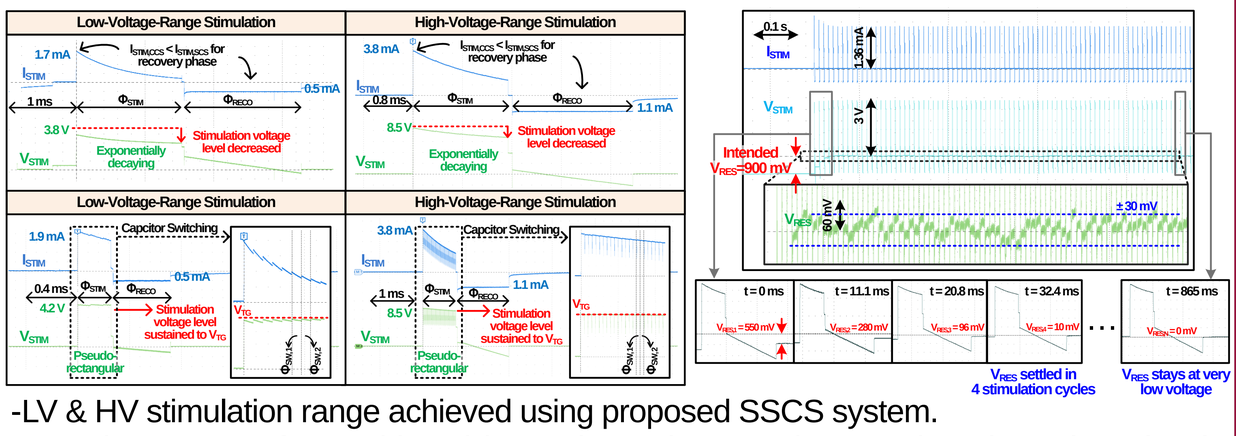
-Process: 250nm CMOS
-Chip Area: 3.45 x 3.90 mm^2

• **Measured Efficiency**



-Max. charging efficiency of 72.6% (1μF cap from 0 to 4V)
-Discharging efficiency is load dependent (96.5% - 99.9%)

• **Verification**



-LV & HV stimulation range achieved using proposed SSCS system.
-Pseudo-rect. waveform achieved (LV and HV stim. range) & sustains stim. voltage level.
-Intended residual voltage of 900mV suppressed to 10mV in only 4 stim. cycles.

Performance Summary & Comparison

Publication	JSSC 2018 [5]	CICC 2022 [1]	SSCL 2022 [4]	TBCAS 2016 [3]	JSSC 2022 [6]	This Work
Technology	0.35-μm HV CMOS	0.18-μm CMOS	0.18-μm CMOS	0.18-μm CMOS	0.18-μm HV CMOS	0.25-μm CMOS
Stimulator Type	CCS	SCS	CCS (Discrete)	CCS	CCS	Stacked-SCS [A]
Core Chip Area	1.94 mm^2	1.28 mm^2	1.77 mm^{2B}	0.51 mm^{2B}	30.25 mm^2	10.34 mm^2
# Channels	1	4	16	1	16	4
HV Supply for Stimulus	22 V (External)	3.3 V	3.3 - 12 V (Charge Pump)	0 - 12 V (External)	40 V (Charge Pump)	Not Required (Stacked Capacitors)
HV Tolerant w/ LV Process	Partially	No	Yes	Yes	No	Yes
Stimulation Amplitude	0.001 - 5.12 mA	0 – 3 V	0.1 - 1 mA	0.2 - 3 mA	12.75 mA	0 - 9 V (6bit)
Charging Efficiency	N/A	90% (0→3 V) DC-to-Cap.	N/A	N/A	N/A	72.6% (0→4 V) AC-to-Cap.
Discharging Efficiency	N/A	99.2% (1kΩ)	N/A	N/A	N/A	96.5 - 99.9% (2.2 - 10.1 kΩ)
Stimulator Efficiency	23.3% (5.12 mA, 1 kΩ)	89.3% (3 V, 1 kΩ)	60% [C]	37%	31.9%	71.4% (4 V, 2.2 kΩ)
Stimulus Shape	Rectangular	Decaying Exponential	Rectangular	Rectangular	Rectangular	Decaying Exponential & Pseudo-Rectangular
Stimulation Pulse Width	N/A	250 - 2000 μs	External Ctrl.	N/A	N/A	128 - 1920 μs
Stimulation Frequency	N/A	75 - 250 Hz	External Ctrl.	N/A	N/A	100 - 1100 Hz
CB Method	Pulse Insertion & Offset Control	Amplitude Offset Controlled	N/A	Bipolar Matching	Pulse Insertion	Stimulus-Synchronized Pulse-Width Control
Need for Additional CB Period	No	Yes	N/A	Yes	No	No
Residual Voltage	20 mV	90 mV	N/A	118.9 mV	2 mV	< 30 mV
Settling Time	N/A	N/A	N/A	Shorted @ 10 Stimulation Cycles	Linear (I_{PT}= 0.2 mA)	Self-adaptive < 4 Stimulation Cycles [D]

[A] SSCS for stimulation phase and CCS for recovery phase [B] Discrete devices not included [C] Estimated [D] Time taken to remove 900mV intended V_{RES}

Acknowledgement
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